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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/636,108	08/07/2003	Tatsuya Inoue	MAT-8437US	1573

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EXAMINER	
PHU, SANH D	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 04/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/636,108	INOUE ET AL.	
	Examiner	Art Unit	
	Sanh D. Phu	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/8/05*., 8 17 10 3
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 12/08/05 and 8/7/03. The information disclosure statements are considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4, 6, 7, 10 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Yokoyama et al (5,375,256), provided by the applicant in the IDS filed on 12/8/05.

-Regarding to claim 1, Yokoyama et al discloses a high-frequency device (see figure 1) comprising:

an antenna terminal (41) (see col. 3, lines 30-34);

a signal line (comprising (43)) connected to said antenna terminal for communicating signals between the antenna terminal and a receiving terminal (46) (see col. 3, lines 30-37, lines 48-51);

a high-frequency signal processing circuit (5, 6, 7) connected to said signal line (see col. 4, lines 6-24);

a capacitance element (42 or 44) having one end connected to said signal line and other end grounded (see figure 1);

and an inductor (45) having one end connected to said signal line and other end grounded.

-Regarding to claim 2, Yokoyama et al discloses that said capacitance element and said inductor are formed integrally with each other within a printed circuit (see figure 3, col. 4, lines 47-60).

-Regarding to claim 4, Yokoyama et al discloses that said capacitance element (42 or 44) is a capacitor (see col. 3, lines 48-59).

-Regarding to claim 6, Yokoyama et al discloses that an inductance of said inductor (45) is about 1.2 nH, namely not larger than 50 nH (see col. 5, lines 60-63).

-Regarding to claim 7, Yokoyama et al discloses that an capacitance of said capacitance element (42) is about 2.5 pF, namely not larger than 10 pF (see col. 5, lines 23-25).

-Regarding to claim 10, Yokoyama et al discloses that said high-frequency signal processing circuit includes a duplexer (5) connected to said signal line (see figure 1).

-Regarding to claim 11, Yokoyama et al discloses that said high-frequency signal processing circuit includes a duplexer/diplexer (5) connected to said signal line (see figure 1). (Note that a duplexer is also known or called

as a diplexer which is a means for allowing the transmit and receive networks to share the same antenna system. For a clarity of this matter, see Mok et al (4,868,575), col. 1, lines 16 and 17).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama et al in view of Killen et al (6,720,926).

-Regarding to claim 3, Yokoyama et al does not teach a ceramic laminated substrate including a ceramic layer and a conductive pattern provided on said ceramic layer, for forming said antenna terminal, said capacitance element, and said inductor, as claimed.

However, Yokoyama et al teaches that said antenna terminal, said capacitance element, and said inductor might be formed by a printed circuit

(considered here equivalent with the limitation "conductive pattern") which is mounted on a printed circuit board (see col. 4, lines 47-51).

Killen et al teaches that a RF circuit can be implemented with a circuit board comprising a surface of an electrically insulating board ceramic substrate on which RF components of the RF circuit are mounted and connected together (see col. 1, lines 60-64).

Since Yokoyama et al does not teach in detail how the printed circuit board is implemented so that the printed circuit can be mounted on, it would have been obvious for a person skilled in the art to implement Yokoyama et al printed circuit board with a circuit board, as taught by Killen et al, in such a way the circuit board comprises a surface of an electrically insulating board ceramic substrate on which said antenna terminal, said capacitance element, and said inductor, formed by the printed circuit, are mounted, so that in Yokoyama et al in view of Killen et al, the printed circuit and printed circuit board would be formed as required.

Therefore, with such the implementation, Yokoyama et al in view of Killen et al teaches the circuit board, (which is considered here equivalent with the

limitation "ceramic laminated substrate") including the surface of the electrically insulating board ceramic substrate, (which is considered here equivalent with the limitation "a ceramic layer") and the printed circuit (considered here equivalent with the limitation "conductive pattern") provided on said ceramic layer, for forming said antenna terminal, said capacitance element, and said inductor, as claimed.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama et al in view of Gupta et al (4,729,058).

-Regarding to claim 5, Yokoyama et al does not discloses that said capacitance element is a varistor.

However, Yokoyama et al discloses said capacitance element is a capacitor (see col. 3, lines 48-59).

Gupta et al teaches that a capacitor can be implemented in such a way that the capacitor will exhibit the characteristics of both a capacitor and a varistor so that the capacitor would have a high voltage surge protection while providing a useful level of capacitance, (see col. 1, lines 61-64, col. 2, lines 60-62).

Since Yokoyama et al does not teach in detail how the capacitor is implemented, it would have been obvious for a person skilled in the art to implement Yokoyama et al capacitor, as taught by Gupta et al, in such a way that the capacitor will exhibit the characteristics of both a capacitor and a varistor so that the capacitor would have a high voltage surge protection while providing a useful level of capacitance as required.

Therefore, with such the implementation, Yokoyama et al in view of Gupta et al teach that the capacitance element is a varistor, as claimed, (because the capacitance element exhibits the characteristics of a varistor).

8. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama et al in view of Rishi (6,127,884).

-Regarding to claim 8, Yokoyama et al does not discloses that said high-frequency signal processing circuit includes a switch connected to said signal line, as claimed.

Yokoyama discloses that said high-frequency signal processing circuit includes a duplexer (5) connected to said signal line (see figure 1) for allowing

transmit section (6) and receive section (7) to share the same antenna (ANTENNA).

Rishi teaches that either one of a duplexer or a switch can be alternatively selected to be employed for allowing the transmit and receive networks to share the same antenna system (see (5) of figure 1, and col. 3, lines 24-32).

Therefore, it would have been obvious for a person skilled in art, in an alternative way as taught by Rishi, to replace Yokoyama et al duplexer with a switch so that in Yokoyama et al in view of Rishi, the switch would allow the transmit section (6) and receive section (7) to share the same antenna (ANTENNA) as required.

-Regarding to claim 9, as applied to claim 8, Yokoyama et al implementation in view Rishi does not teaches said high-frequency signal processing circuit includes a filter connected to said switch, as claimed.

However, Yokoyama et al in view of Rishi, teaches that in said high-frequency signal processing circuit, said switch (in place of duplexer (5)) is coupled the transmit section (6) (see Yokoyama et al, figure 1).

Rishi teaches a filter (28) connected to such a switch for coupling a transmit section (2) to the switch for filtering signal outputted from the transmit section before it being inputted to the switch (see figure 1, and col. 3, lines 51-53).

Since Yokoyama et al does not teach in detail how the transmit section (6) is implemented, it would have been obvious for a person skilled in the art to implement the transmit section (6) of said high-frequency signal processing circuit, in Yokoyama et al in view of Rishi, with a filter, as taught by Rishi, in such a way that the filter would couple the transmit section (6) (see Yokoyama et al, figure 1) to the said switch (in place of duplexer (5)) (see Yokoyama et al, figure 1) so that undesired signals would be filtered from the output signal outputted from the transmit section by the filter before the output signal being inputted to the switch for further transmission.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mok et al (4,868,575) is additionally cited because it is pertinent to the claimed subject matter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sanh D. Phu whose telephone number is (571)272-7857. The examiner can normally be reached on M-Th from 7:00-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew D. Anderson can be reached on (571) 272-4177. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sanh D. Phu
Examiner
Division 2618

SP

4/14/06

SANH D. PHU
PATENT EXAMINER